



PDFN/PPAK5×6-8L Plastic-Encapsulate MOSFETS

CCME130N04S N-Channel Power MOSFET

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D
40 V	1.6mΩ@10V	130A
	2.3mΩ@4.5V	

DESCRIPTION

The CCME130N04S uses advanced SGT technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications .

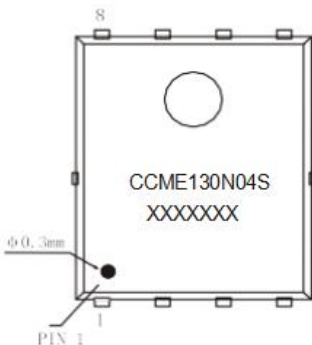
FEATURES

- Power MOSFET for automotive applications
- 100% Avalanche tested
- 175°C operating temperature
- Green Product(RoHS compliant)
- AEC Q101 qualified

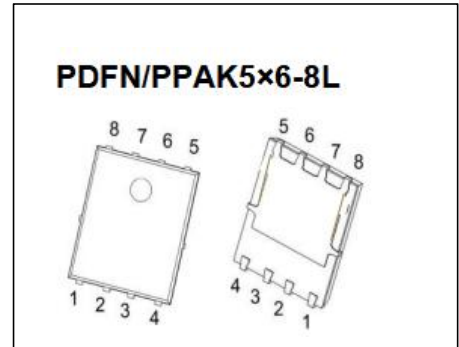
APPLICATIONS

- Electronic water pump
- Electric steering
- ESC

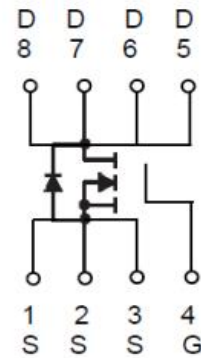
MARKING



CCME130N04S =Part No.
XXXXXXX = Code.



EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS($T_c=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ¹	I_D	130	A
Pulsed Drain Current ²	I_{DM}	520	A
Single Pulse Avalanche Energy ³	EAS	400	mJ
Total Power Dissipation ¹	P_D	83	W
Thermal Resistance from Junction to Case ¹	$R_{\theta JC}$	1.8	$^{\circ}\text{C}/\text{W}$
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55~ +175	$^{\circ}\text{C}$
Soldering Temperature , for 10S(1.6mm from case)	-	260	$^{\circ}\text{C}$

Notes:

1. Current is limited by package; with a $R_{thjc} = 1.8^{\circ}\text{C}/\text{W}$ the chip is able to carry 184 A at 25°C .
2. $P_w \leq 10\mu\text{s}$, Duty cycle $\leq 1\%$.
3. EAS condition: $V_{DD}=20\text{V}, V_{GS}=10\text{V}, I_D=40\text{A}, L=0.5\text{mH}, R_g=25\Omega$ Starting $T_J = 25^{\circ}\text{C}$.

MOSFET ELECTRICAL CHARACTERISTICS

TC=25°C unless otherwise specified

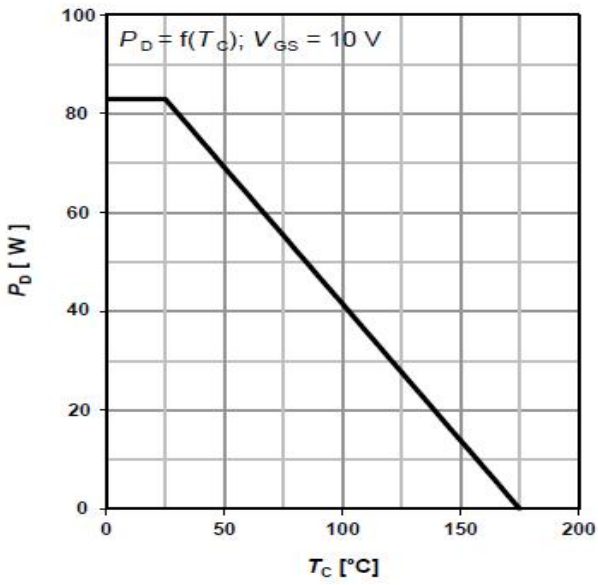
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Off characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	40			V
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 40V, V_{GS} = 0V$	$T_J = 25^\circ C$		1	μA
			$T_J = 125^\circ C$		100	
Gate-body leakage current	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 100	nA
On characteristics⁴						
Gate-threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.5	1.7	2.2	V
Static drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 60A$		1.6	2.0	m Ω
			$V_{GS} = 4.5V, I_D = 20A$		2.3	2.8
Forward transconductance	g_{fs}	$V_{DS} = 10V, I_D = 10A$		95		S
Dynamic characteristics³⁴						
Input capacitance	C_{iss}	$V_{DS} = 25V, V_{GS} = 0V, f = 1MHz$		3730	4850	μF
Output capacitance	C_{oss}			1019	1325	
Reverse transfer capacitance	C_{rss}			62	81	
Gate resistance	R_g	$f = 1MHz$		2.2		Ω
Switching characteristics³⁴						
Total gate charge	Q_g	$V_{GS} = 0-10V, V_{DD} = 32V, I_D = 130A$		52		nC
Gate-source charge	Q_{gs}			28		
Gate-drain charge	Q_{gd}			16		
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 20V, I_D = 130A, V_{GS} = 10V, R_G = 3.5\Omega$		15		ns
Turn-on rise time	t_r			18		
Turn-off delay time	$t_{d(off)}$			55		
Turn-off fall time	t_f			30		
Drain-Source Diode Characteristics						
Drain-source diode forward voltage ⁴	V_{SD}	$V_{GS} = 0V, I_S = 60A$			1.2	V
Continuous drain-source diode forward Current ¹	I_S	-			130	A
Pulsed drain-source diode forward current ²	I_{SM}	-			520	A
Reverse recovery time	T_{rr}	$I_F = 60A, di/dt = 100A/\mu s$			50	ns
Reverse recovery charge	Q_{rr}				38	nC

Note :

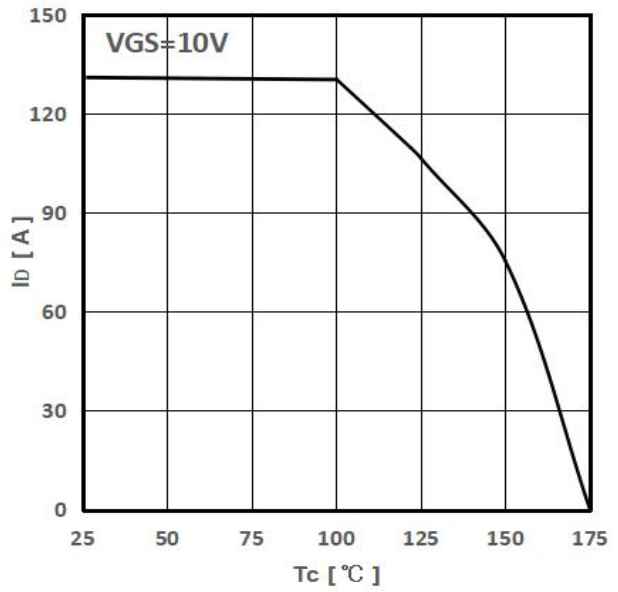
1. Current is limited by package; with a $R_{thjc} = 1.8^\circ C/W$ the chip is able to carry 184A at 25°C.
2. $P_W \leq 10\mu s$, Duty cycle $\leq 1\%$.
3. Guaranteed by design, not subject to production.
4. Pulse Test : Pulse Width $\leq 400\mu s$, duty cycle $\leq 2\%$.

Typical Characteristics

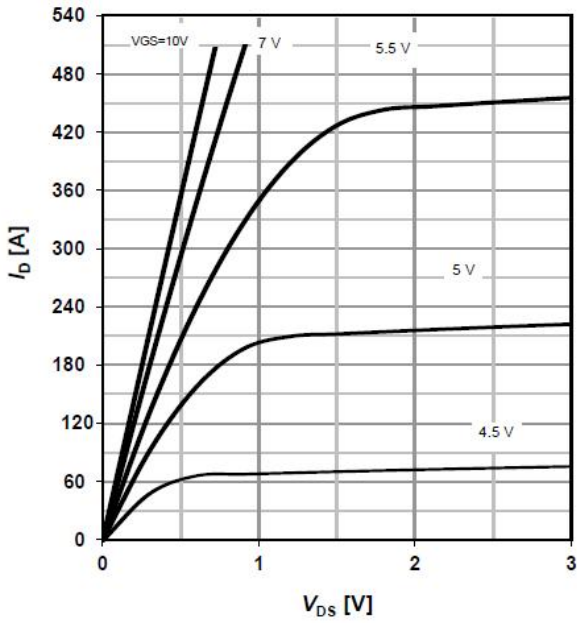
PD -- Tc



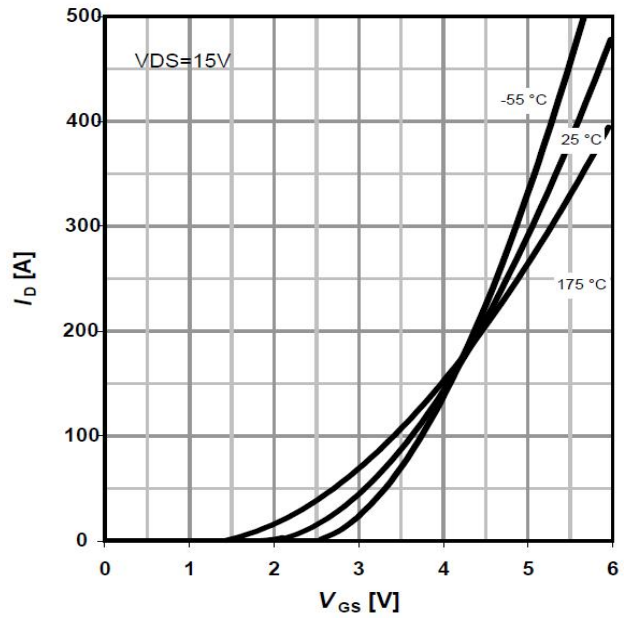
ID -- Tc



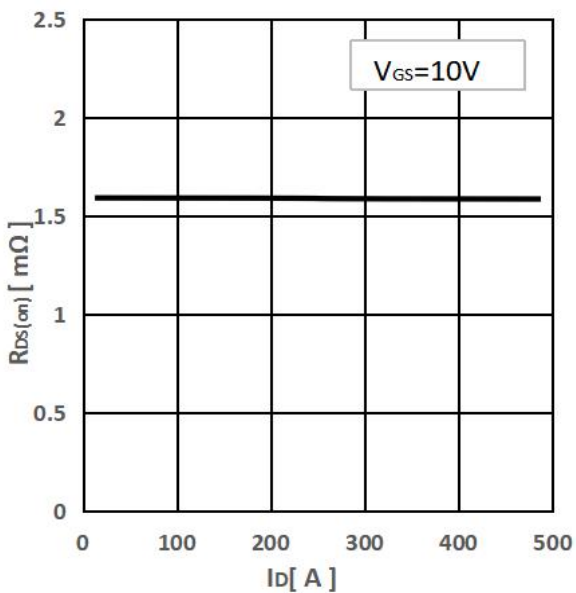
ID -- VDS



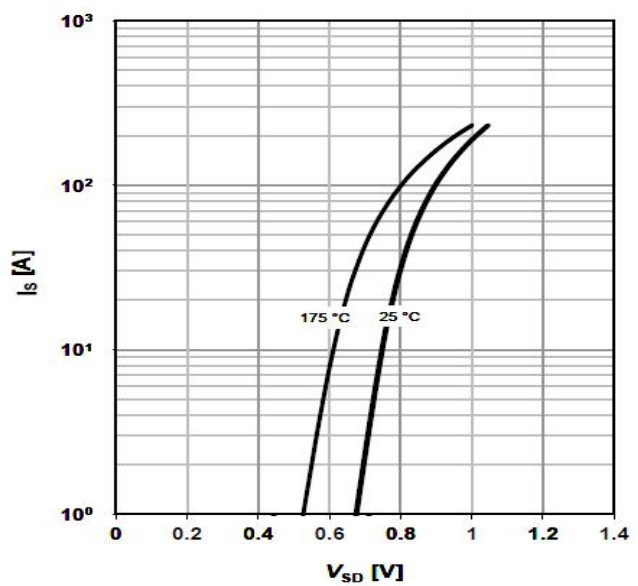
ID -- VGS



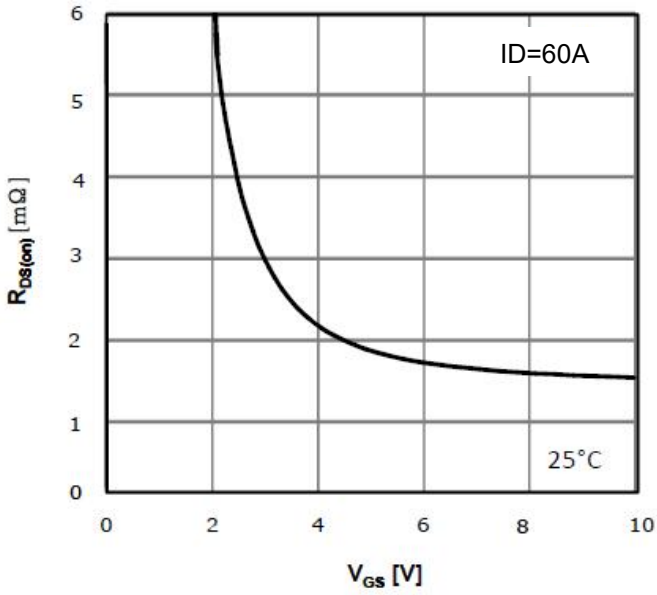
RDS(on) -- ID



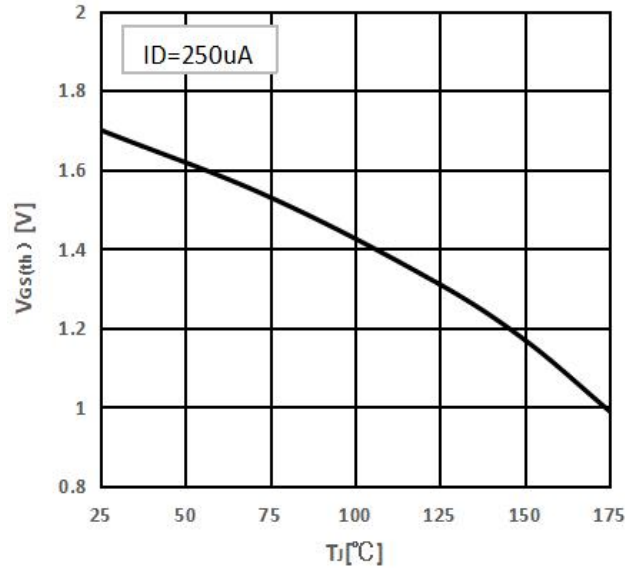
IS -- VSD



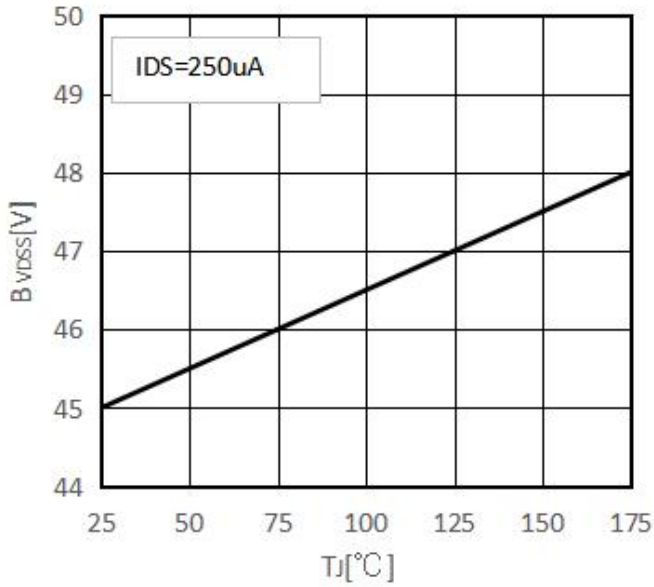
RDS(on) -- VGS



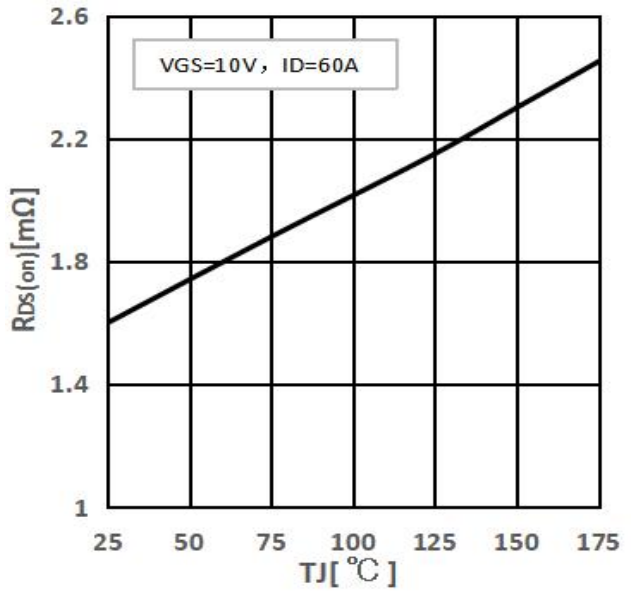
Threshold Voltage



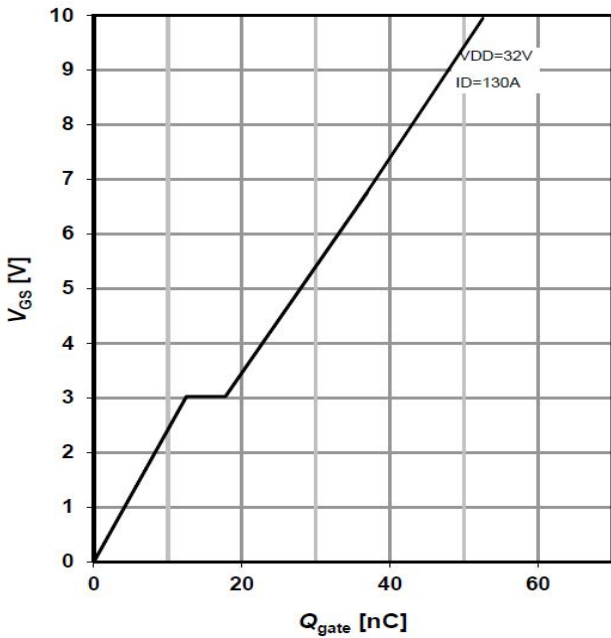
Drain-source breakdown voltage



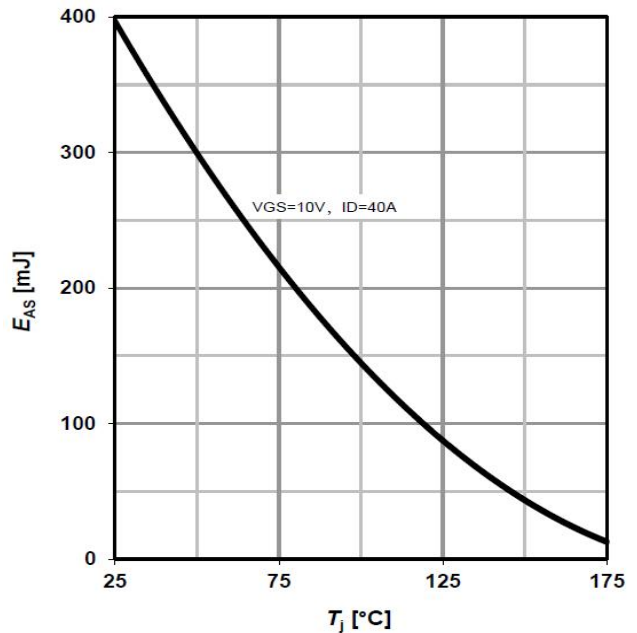
RDS (on) -- TJ



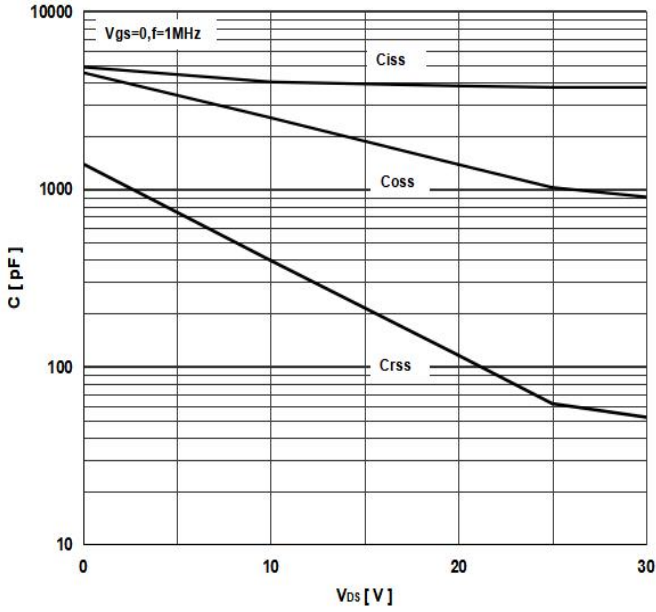
Typ.gate charge



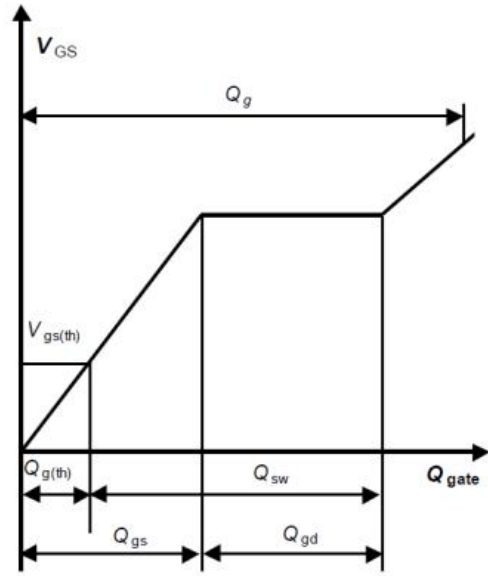
Avalanche energy



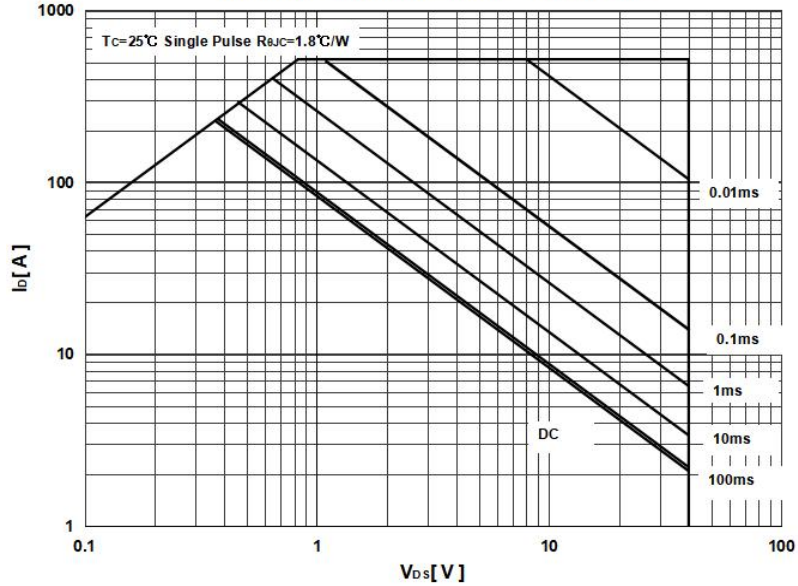
Typ. capacitance



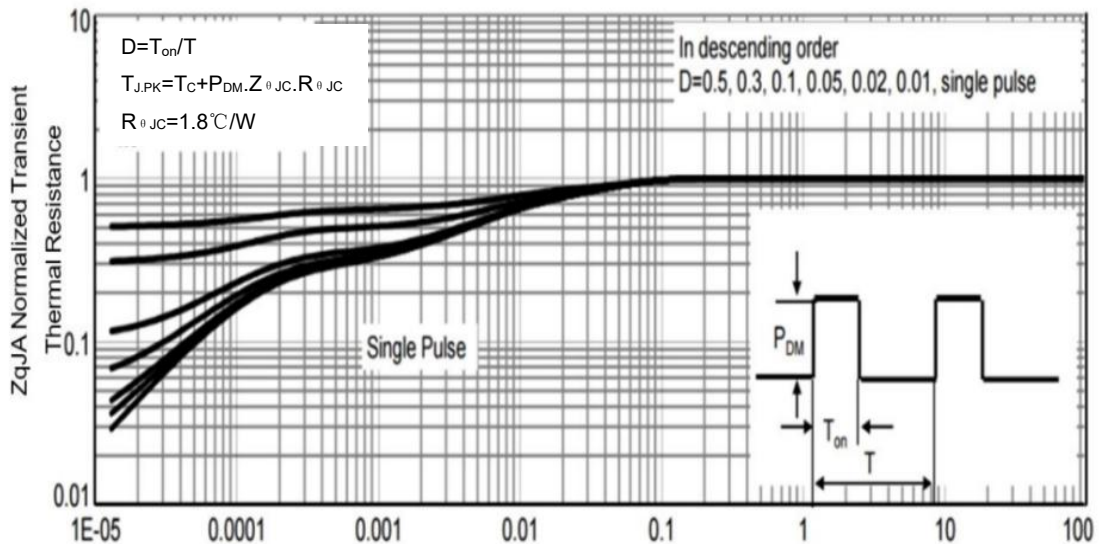
Gate charge waveforms



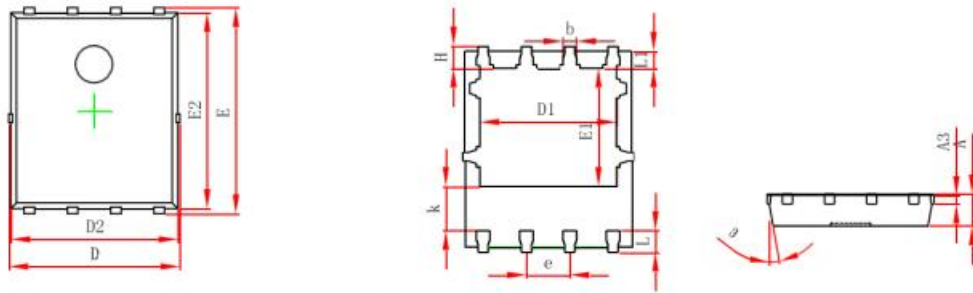
Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance

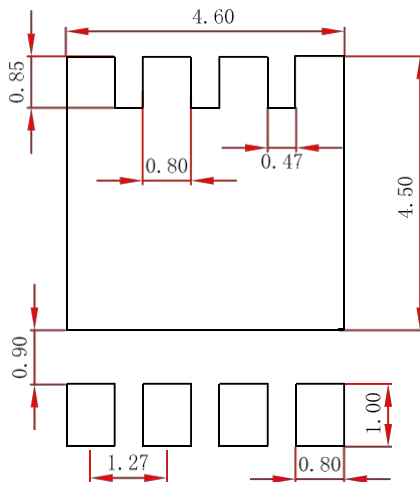


PDFN/PPAK5*6-8L Package Outline Dimensions



Symbol	Dimension in Millimeters		Dimension in Inches	
	Min	Max	Min	Max
A	0.950	1.150	0.037	0.045
A3	0.200	0.300	0.008	0.012
D	4.950	5.350	0.195	0.211
E	5.950	6.350	0.234	0.250
D1	3.900	4.200	0.154	0.165
E1	3.380	3.730	0.133	0.147
D2	4.900	5.300	0.193	0.209
E2	5.700	5.900	0.224	0.232
k	1.180	1.480	0.046	0.058
b	0.350	0.450	0.014	0.018
e	1.220	1.320	0.048	0.052
L	0.500	0.700	0.020	0.028
L1	0.325	0.575	0.013	0.023
H	0.500	0.700	0.020	0.028
θ	10°	12°	10°	12°

PDFN/PPAK5*6-8L Suggested Pad Layout



Note:

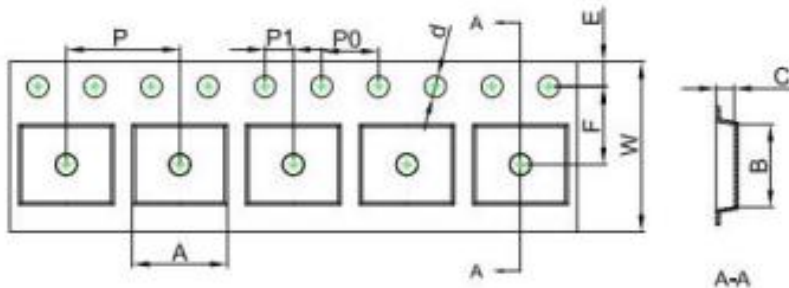
1. Controlling dimension: in millimeters.
2. General tolerance: 0.5mm.
3. The pad layout is for reference purposes only.

NOTICE

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PDFN/PPAK5*6-8L Embossed Carrier Tape

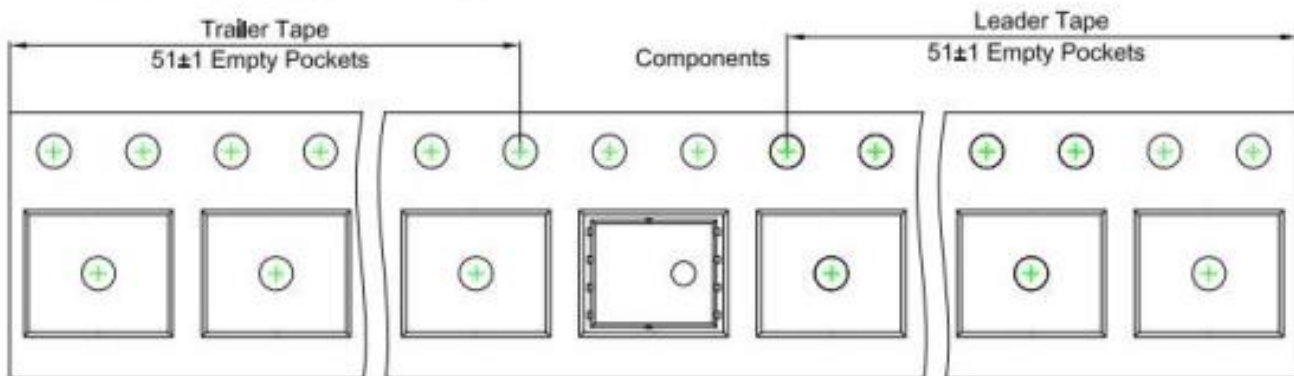


Packaging Description:

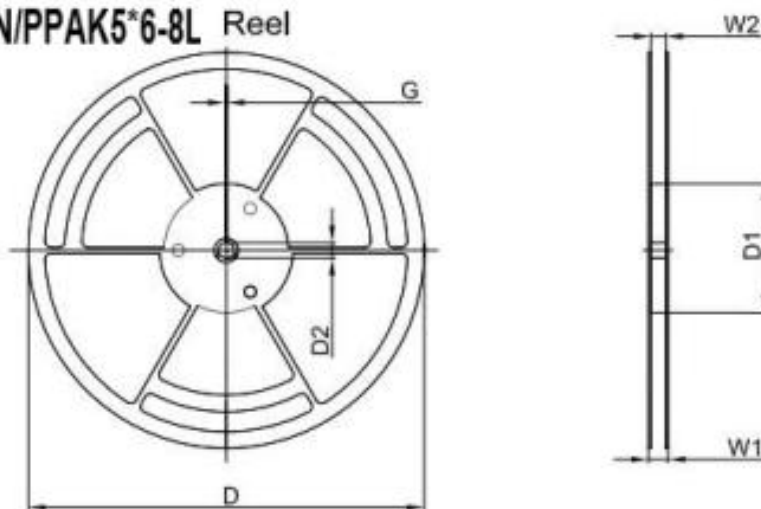
PDFN/PPAK5*6-8L parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 5,000 units per 13" or 33,0 cm diameter reel. The reels are clear in color and is made of polystyrene plastic (anti-static coated).

Dimensions are in millimeter										
Pkg type	A	B	C	d	E	F	P0	P	P1	W
PDFN/PPAK5*6-8L	6,30	5,30	1,10	Ø1,50	1,75	5,50	4,00	8,00	2,00	12,00

PDFN/PPAK5*6-8L Tape Leader and Trailer



PDFN/PPAK5*6-8L Reel



Dimensions are in millimeter						
Reel Option	D	D1	D2	G	W1	W2
13"Dia	Ø330,00	100,00	13,00	1,90	17,80	12,40

REEL	Reel Size	Box	Box Size(mm)	Carton	Carton Size(mm)
5,000 pcs	13 inch	5,000 pcs	340×336×29	50,000 pcs	353×346×365

Date of change	Rev #	revise content
2022/11/24	A/0	/
2024/01/05	A/1	微调产品实测参数（提高测试电流），增加结电容上限