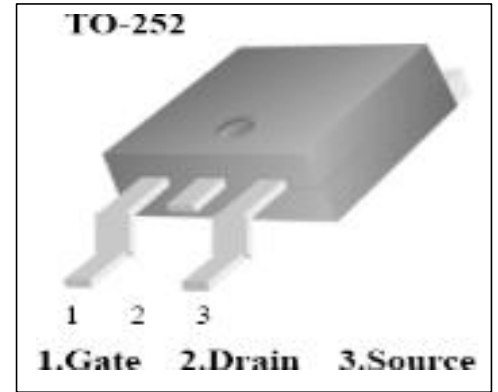




TO-252 Plastic-Encapsulate MOSFETS

CR4N65 A4K N-Channel Power MOSFET

V_{DSS}	$R_{DS(ON)}$ (Typ.)	I_D
650 V	2.4 Ω @10V	4A



DESCRIPTION

The CR4N65 A4K provides excellent $R_{DS(ON)}$ with low gate charge.

It can be used in a wide variety of applications.

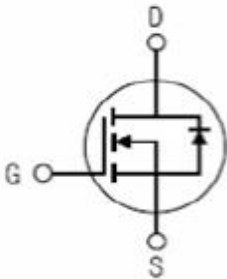
FEATURES

- Fast Switching
- Low Gate Charge
- Low ON Resistance
- Low Reverse transfer capacitances
- 100% Single Pulse avalanche energy Test
- AEC-Q101 Qualified

APPLICATIONS

- Power switch circuit of adaptor and charger.

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS($T_J=25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain - Source Voltage	V_{DS}	650	V
Gate - Source Voltage	V_{GS}	± 30	V
Continuous Drain Current ¹	I_D	4	A
$T_A = 25^{\circ}\text{C}$			
Pulsed Drain Current ²	I_{DM}	16	A
Power Dissipation ⁴	P_D	90	mW
$T_A = 25^{\circ}\text{C}$			
Thermal Resistance from Junction to Case	$R_{\theta JA}$	1.67	$^{\circ}\text{C}/\text{W}$
Junction Temperature	T_J	175	$^{\circ}\text{C}$
Storage Temperature	T_{STG}	-55~ +175	$^{\circ}\text{C}$
Single Pulse Avalanche Energy ⁵	E_{AS}	200	mJ

MOSFET ELECTRICAL CHARACTERISTICS($T_C=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Off Characteristics						
Drain – Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu\text{A}$	650			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 650V, V_{GS} = 0V$			1	μA
Gate – Body Leakage Current	I_{GSS}	$V_{GS} = \pm 30V, V_{DS} = 0V$			± 100	nA
On Characteristics³						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	2.0		4.0	V
Drain-source On-resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 2A$		2.4	2.8	Ω
Dynamic Characteristics						
Input Capacitance	C_{iss}	$V_{DS} = 25V, V_{GS} = 0V, f = 1\text{MHz}$		564		pF
Output Capacitance	C_{oss}			41		
Reverse Transfer Capacitance	C_{rss}			2.4		
Forward Transconductance	g_{fs}	$V_{DS} = 15V, I_D = 2A$		3.5		S
Switching Characteristics						
Total Gate Charge	Q_g	$V_{DS} = 520V, V_{GS} = 10V, I_D = 4A$		15.8		nC
Gate-source Charge	Q_{gs}			3.0		
Gate-drain Charge	Q_{gd}			8.5		
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 325V, V_{GS} = 10V,$ $R_G = 10\Omega, I_D = 4A$		13		ns
Turn-on Rise Time	t_r			9		
Turn-off Delay Ttime	$t_{d(off)}$			24		
Turn-off Fall Ttime	t_f			10		
Source - Drain Diode Characteristics						
Diode Forward Voltage ³	V_{SD}	$V_{GS} = 0V, I_S = 4A$			1.5	V

Notes :

- The maximum current rating is limited by Chip.
- Repetitive rating; pulse width limited by maximum junction temperature
- Pulse Test : Pulse Width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
- The power dissipation PD is limited by $T_{J(MAX)} = 175^{\circ}\text{C}$.
- $L=10\text{mH}, I_D=6.3A, T_J=25^{\circ}\text{C}$.

Characteristics Curve:

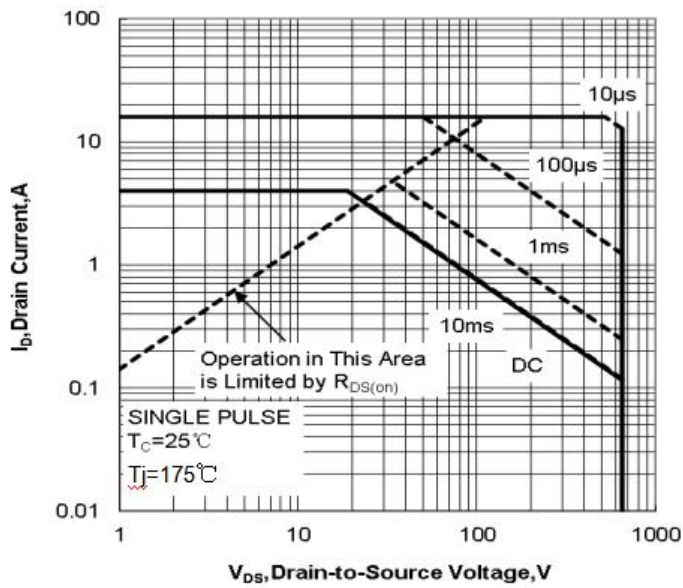


Figure.1 Maximum Forward Bias Safe Operating Area

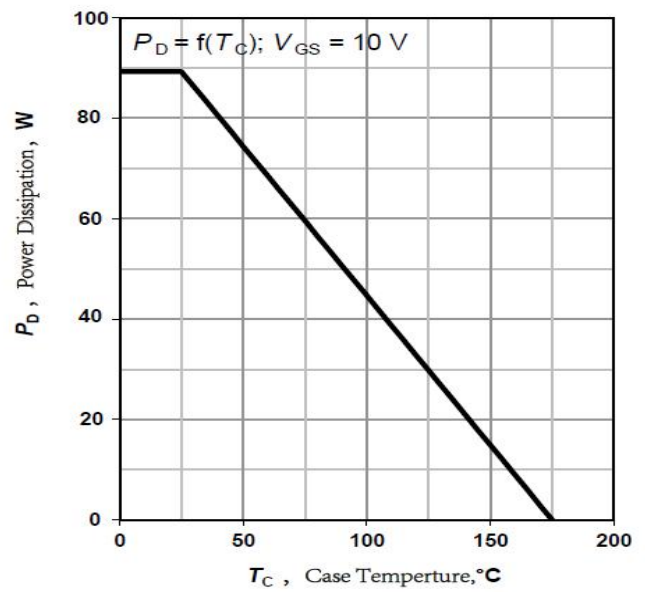


Figure.2 Maximum Power Dissipation vs Case Temperature

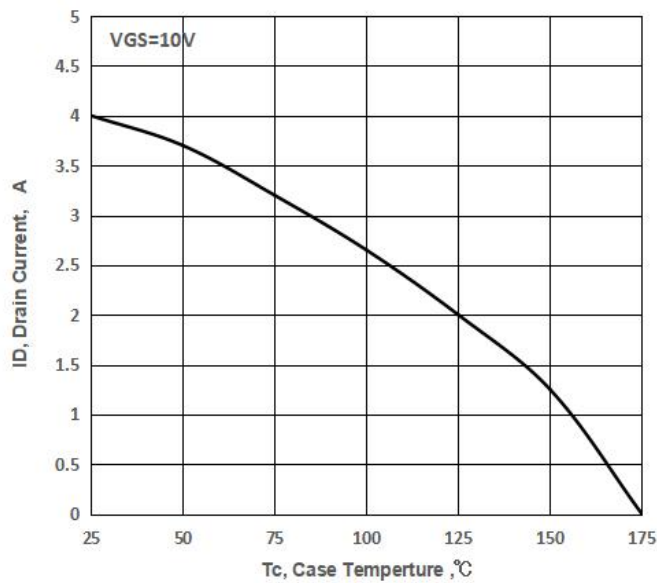


Figure.3 Maximum Continuous Drain Current vs Case Temperature

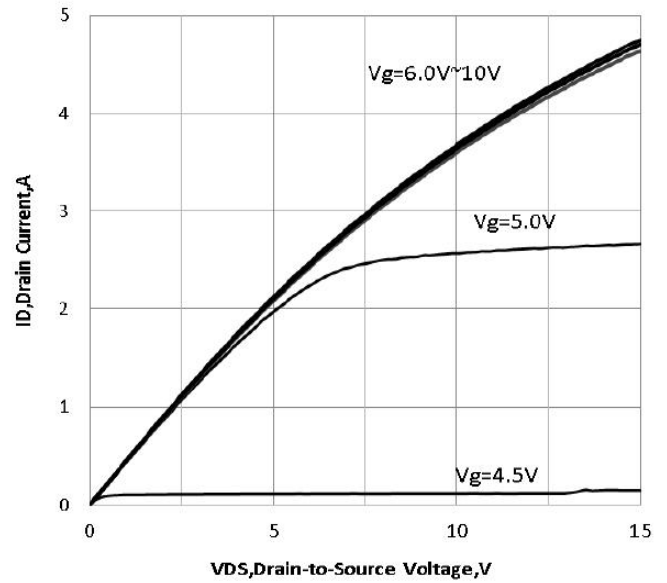


Figure.4 Typical Output Characteristics

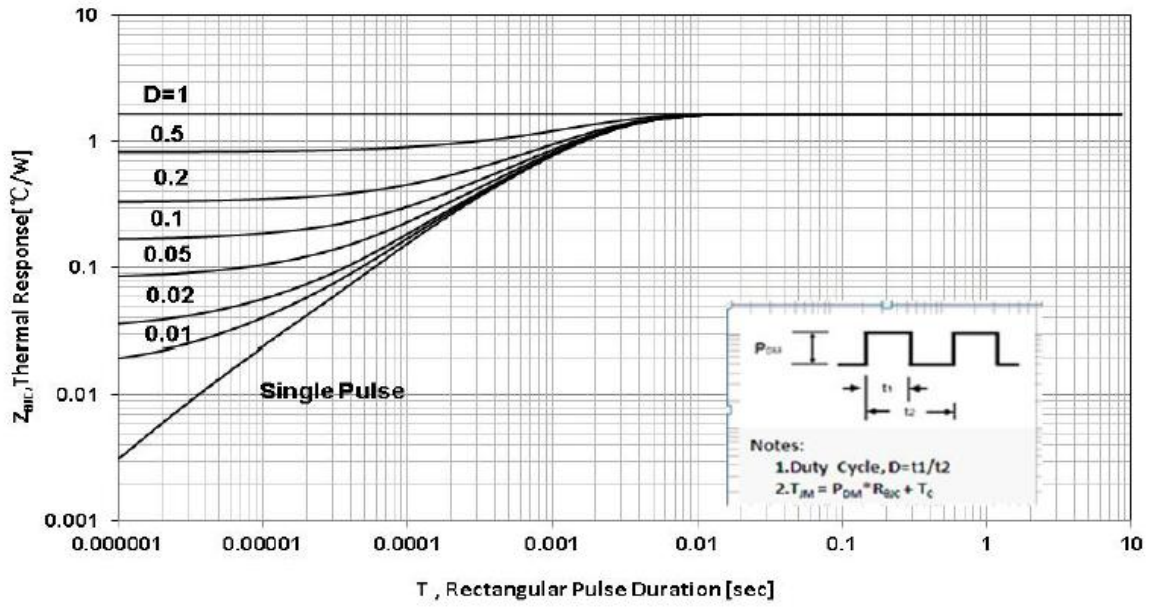


Figure.5 Maximum Effective Thermal Impedance , Junction to Case

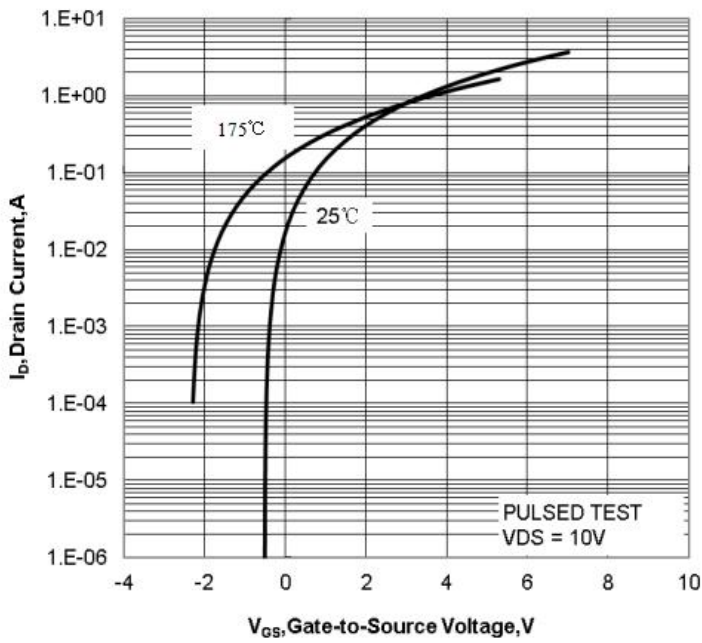


Figure.6 Typical Transfer Characteristics

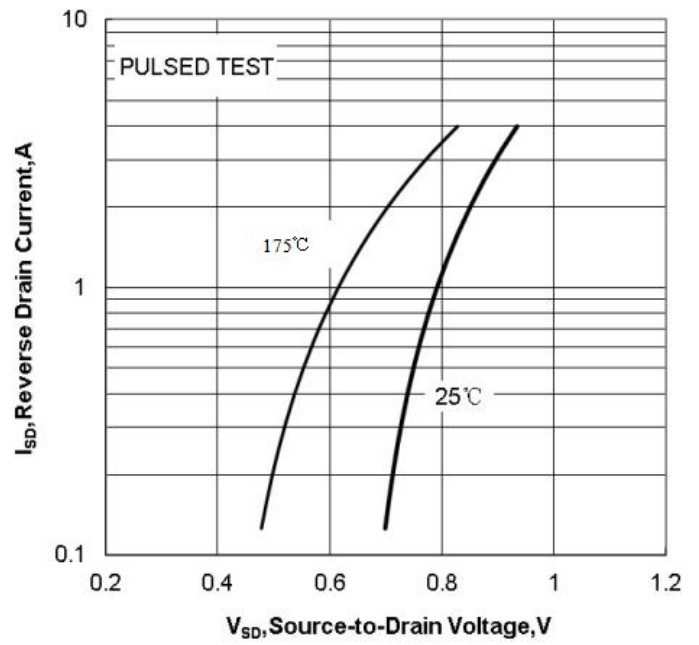


Figure.7 Typical Body Diode Transfer Characteristics

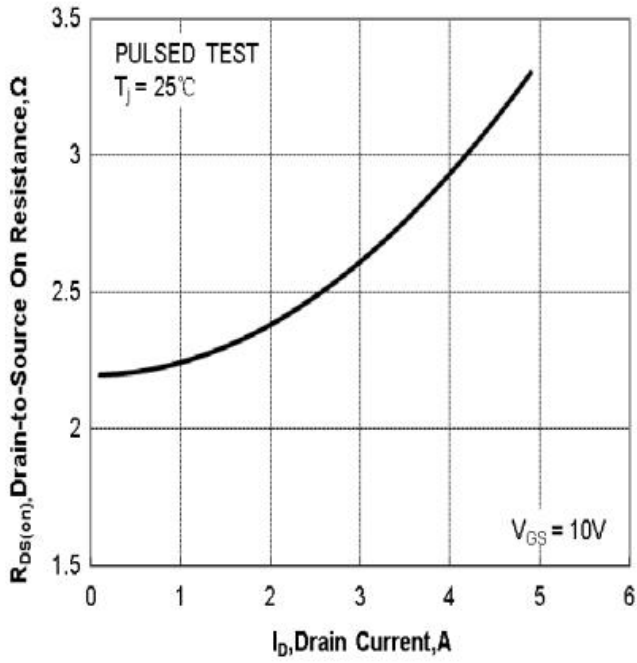


Figure.8 Typical Drain to Source ON Resistance vs Drain Current

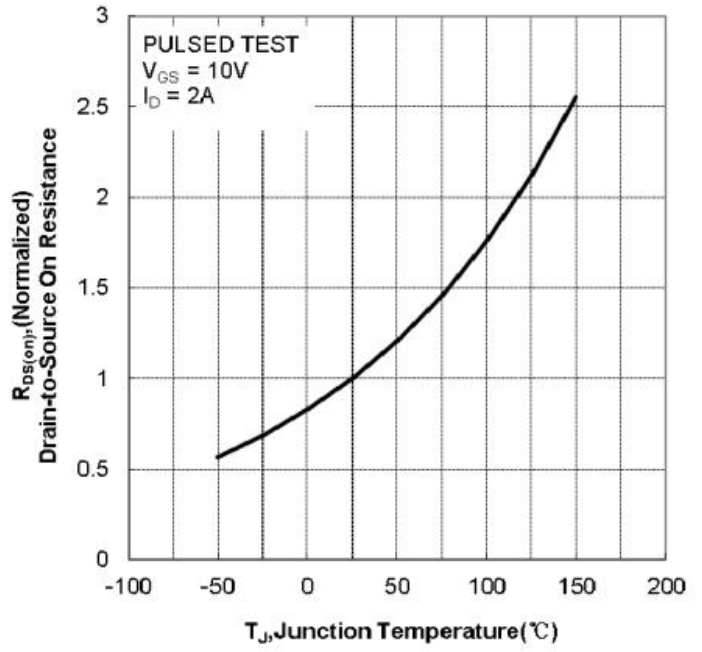


Figure.9 Typical Drain to Source on Resistance vs Junction Temperature

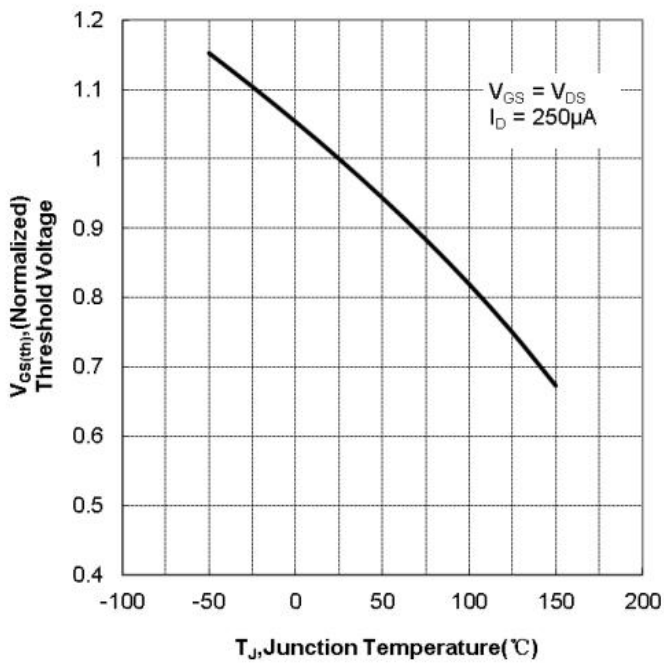


Figure.10 Typical Threshold Voltage vs Junction Temperature

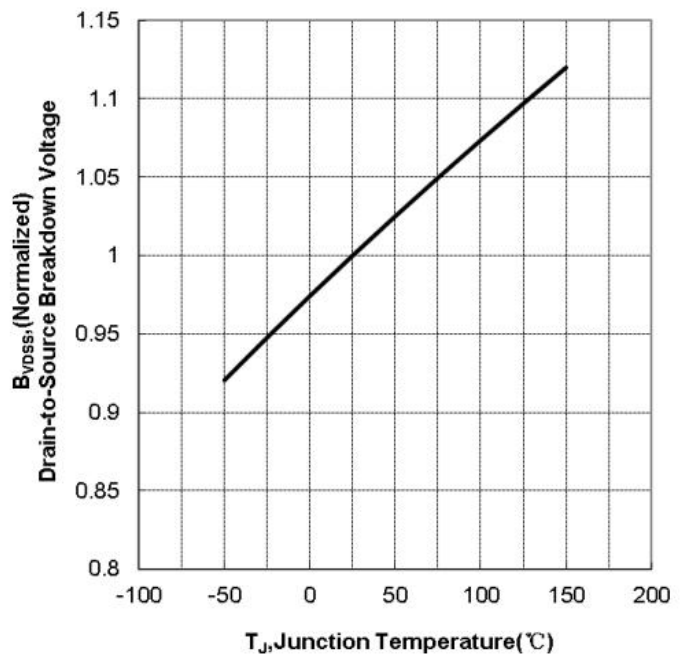


Figure 11 Typical Breakdown Voltage vs Junction Temperature

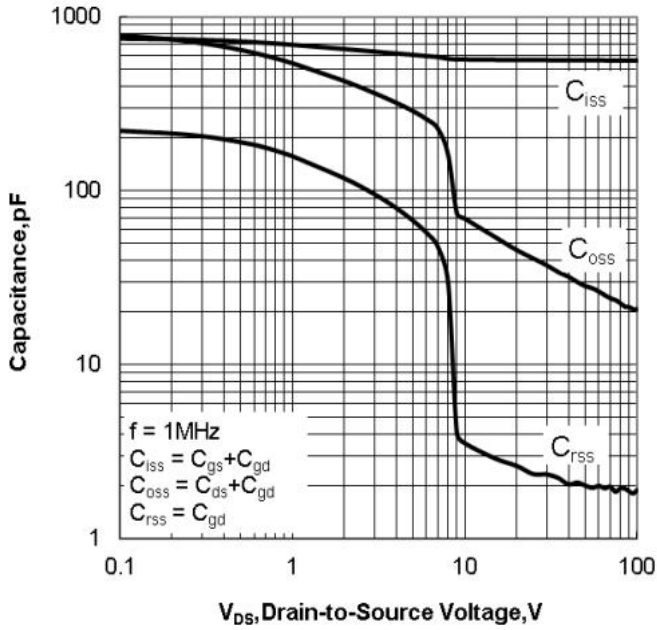


Figure.12 Typical Capacitance vs Drain to Source Voltage

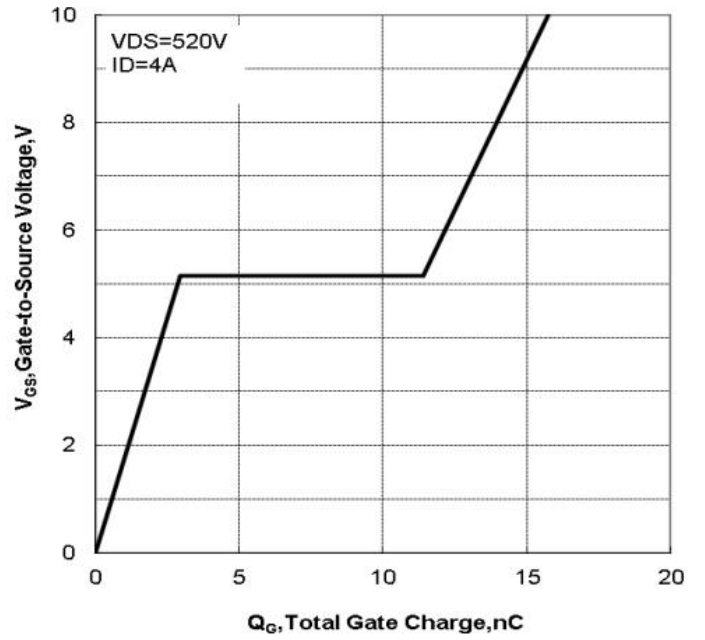


Figure.13 Typical Gate Charge vs Gate to Source Voltage

Test Circuit and Waveform

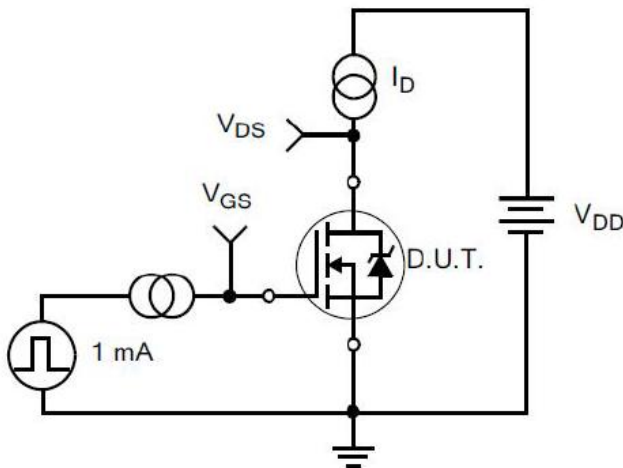


Figure 14. Gate Charge Test Circuit

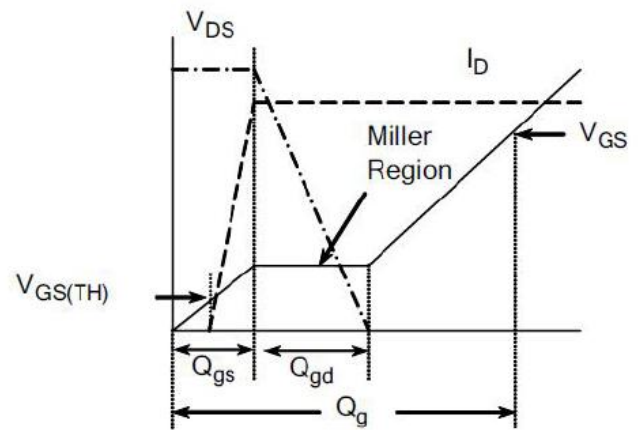


Figure 15. Gate Charge Waveforms

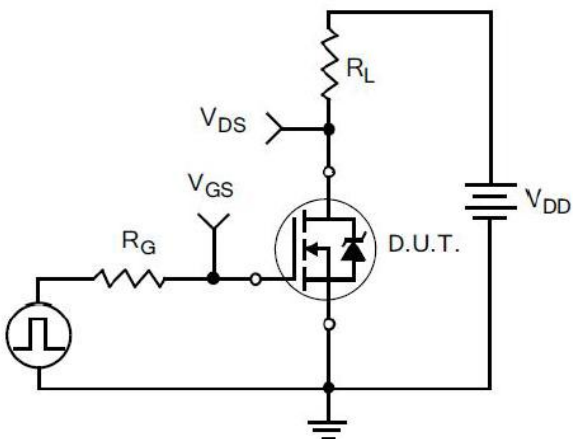


Figure 16. Resistive Switching Test Circuit

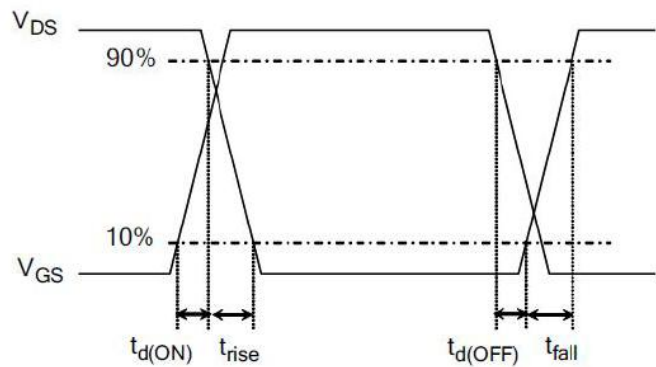


Figure 17. Resistive Switching Waveforms

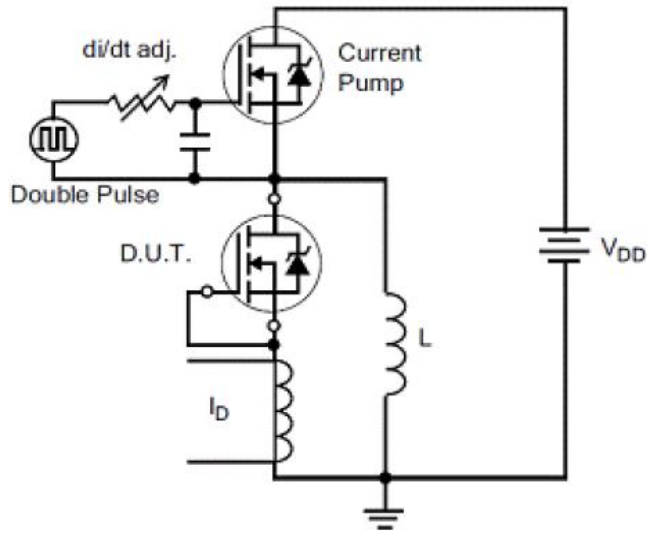


Figure 18. Diode Reverse Recovery Test Circuit

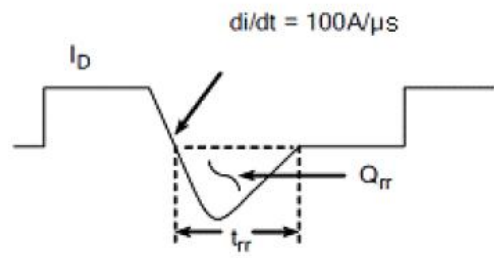


Figure 19. Diode Reverse Recovery Waveform

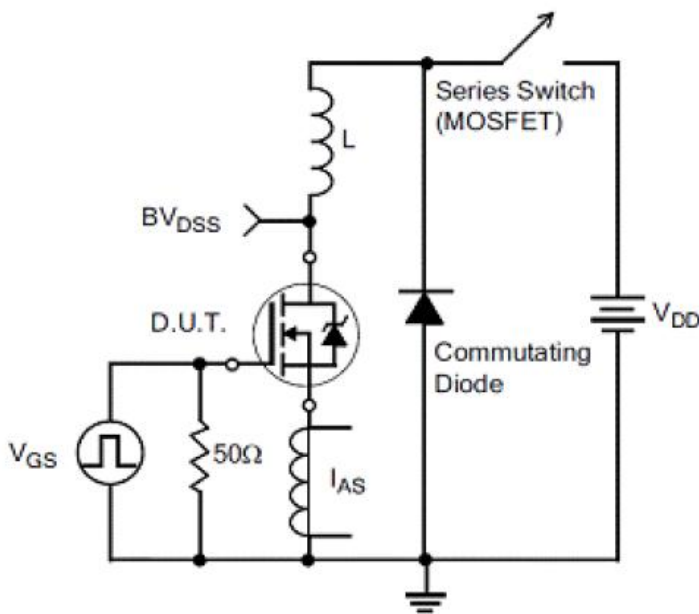


Figure20.Unclamped Inductive Switching Test Circuit

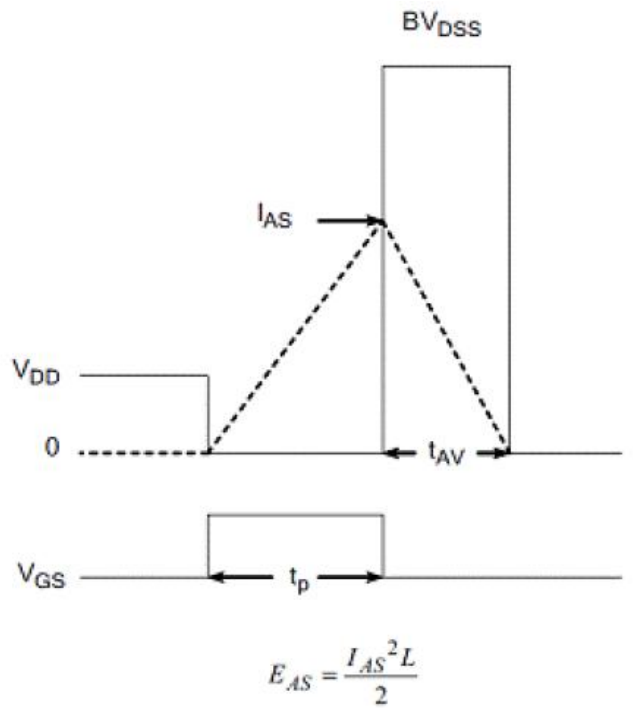
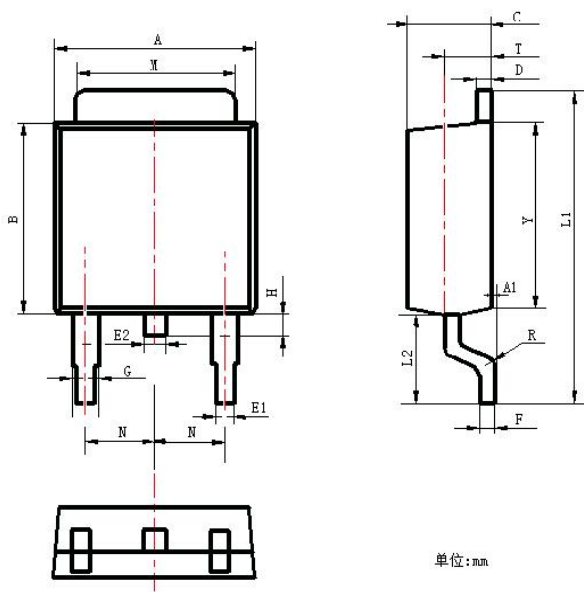


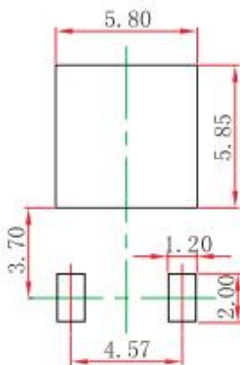
Figure21.Unclamped Inductive Switching Waveform

TO-252 Package Outline Dimensions



Items	Values(mm)	
	MIN	MAX
A	6.30	6.90
A1	0	0.16
B	5.70	6.30
C	2.10	2.50
D	0.30	0.70
E1	0.60	0.90
E2	0.70	1.00
F	0.30	0.60
G	0.70	1.20
L1	9.60	10.50
L2	2.70	3.10
H	0.40	1.00
M	5.10	5.50
N	2.09	2.49
R	0.3	
T	1.40	1.60
Y	5.10	6.30

TO-252 Suggested Pad Layout



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: 0.5mm.
3. The pad layout is for reference purposes only.

NOTICE

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Date of change	Rev #	revise content
2023/2/27	A/0	/